

Optimization of passivation in AlGaIn/GaN heterostructure microwave transistor fabrication by ICP CVD

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Abstract

We have studied the effect of silicon nitride (SiN) dielectric passivating film deposition by inductively coupled plasma chemical vapor deposition (ICP CVD) on the parameters of AlGaIn/GaN heterostructure high electron mobility transistors (HEMT). Study of the parameters of the dielectric layers has allowed us to determine the effect of RF and ICP power and working gas flow ratio on film growth rate and structural perfection, and on the current vs voltage curves of the passivated HEMT. The deposition rate changes but slightly with an increase in RF power but increases with an increase in ICP power. Transistor slope declines considerably with an increase in RF power: it is the greatest at minimum power RF = 1 W. In the beginning of growth even at a low RF power (3 W) the transistor structure becomes completely inoperable. Dielectric deposition for HEMT passivation should be started at minimum RF power. We have developed an AlGaIn/GaN microwave HEMT passivation process providing for conformal films and low closed transistor drain-source currents without compromise in open state transistor performance: within 15 and 100 mA, respectively, for a 1.25 and 5 mm common T-gate ($U_g = -8$ V and $U_{ds} = 50$ V).

Keywords

silicon nitride, plasmachemical deposition, ICP CVD, AlGaIn/GaN HEMT, passivation, current-voltage curves

1. Introduction

Significant progress has been achieved nowadays in the development of AlGaIn/GaN heterostructure and device technologies. These devices have been put into mass production in the last decade. The interest to this technology is aroused primarily by the unique performance of the AlGaIn/GaN material, e.g. high electron mobility in 2D electron gas, high electron drift saturation velocity, high radiation and temperature resistance and high breakdown

field. The most widely used AlGaIn/GaN heterostructure devices include microwave high electron mobility transistors (HEMT) [1] which can work at high dissipated power and under severe operation conditions.

Currently there the technology of these transistors faces numerous problems one of which is attaining low gate leakage currents and high drain-source breakdown voltages [2]. The leak current depends on several factors, e.g. Schottky barrier inverse thermoelectron emission current [3], bulk trap tunneling current (Frenkel–Poole emission) in the barrier layer and surface leakage current over

surface states [4]. Another fundamental task is avoiding current collapse [5]. Current collapse is caused by carrier trapping in the barrier layer and on the surface [6]. Whereas traps in the barrier layer can be controlled by selecting proper heterostructure growth modes [7, 8], the density of surface states which generate surface traps can be reduced by chemical treatment or passivation.

Typical way to ensure high AlGaN/GaN HEMT breakdown voltage is to increase the gate-drain distance but this increases the open channel resistance R_{ON} . Alternatively to achieve high breakdown voltage one can increase the buffer layer thickness and improve its quality but it should be remembered that growing a thick buffer layer reduces the quality of the interface [9]. Another method of increasing the breakdown voltage is to produce a field plate.

As noted above an efficient tool for handling the above-mentioned problems in AlGaN/GaN HEMT fabrication is surface passivation [10]. Passivating layers for AlGaN/GaN HEMT can be a wide variety of relatively new dielectric materials (Al_2O_3 , HfO_2 and ZrO_2) most of which are produced by atomic layer deposition, as well as dielectrics that are widely used in electronics (SiO_x , SiN_x , SiO_xN_y) [11]. Each material has its advantages and drawbacks: e.g. SiO_x provides for high breakdown voltages but reduces leakage currents but slightly [12]. Dielectric silicon nitride SiN_x films are efficient for reducing leakage currents. Silicon oxinitride SiO_xN_y shows good promise as a passivating layer because it combines the advantages of the two above materials SiO_x and SiN_x [13]. Combinations of passivation coatings are often used.

There are numerous dielectric film deposition methods: PECVD, LPCVD, ICP CVD, ALD etc. [14]. Inductively coupled plasma chemical vapour deposition (ICP CVD) is an improved modification of conventional plasma enhanced chemical vapor deposition (PECVD). In PECVD processes the substrate is put on a heated electrode electrically connected to the chamber chassis. The high-frequency signal (RF power) is applied to the top electrode which is arranged parallel to the substrate and has a gas shower for feeding and distributing the reaction gas mixture. In ICP CVD processes working gases are fed from the top to the ICP source (nitrogen, ammonia or nitrous oxide) and from the adjacent substrate holder (table) of the gas distribution ring (monosilane). The high-frequency signal is applied both to the table (RF power) and to the top coil (ICP power) [15]. ICP power controls the dissociation of working gas molecules and the ion density in the chamber while RF power controls the auto bias voltage on the substrate, i.e., the energy of ions on the specimen. As compared with the PECVD method ICP CVD process allows obtaining high-quality Si_3N_4 and SiO_2 dielectric films at low process temperatures [16–18]. Another advantage of this method is that the plasma formation region is separated from the film deposition region thus minimizing the effect of plasma on the specimen surface [19]. Furthermore the possibility to change deposition mode parameters in an ICP CVD process provides for controlling process conditions and selecting optimum process modes for achieving

the highest quality of the dielectric films [20]. The main deposition parameters influencing the film properties are RF power, ICP power, working gas flow ratio, working pressure and deposition temperature.

The aim of this work is to select the optimum SiN_x dielectric film deposition mode for passivation of diode mesastructures and AlGaN/GaN HEMT T-gates and synthesize passive elements of monolithic integrated circuits.

2. Experimental

Silicon nitride films were deposited on a Oxford Plasma-lab 100 CVD at chamber working pressure $P = 10$ mTorr and temperature $T = 200$ °C. The residual pressure in the chamber before the CVD process was max. $3 \cdot 10^{-7}$ Torr. Other process parameters, e.g. working gas flow ratio, RF and ICP power were varied during the experiment.

The deposited materials were SiH_4/N_2 , the working gas being high purity 6.0 N_2 and high purity 5.0 SiH_4 . In the study of the effect of working power on film parameters the working gas flow ratio was constant: $SiH_4/N_2 = 13.9/13.1$. At this ratio the film composition is close to the stoichiometric one Si_3N_4 (refraction index 2.00). To study the effect of SiH_4 and N_2 flow ratio on film parameters we varied the working gas flow ratio within the following range: monosilane 10.9 to 16.9 scm^3 (standard cubic cm) and nitrogen 16.1 to 10.1 scm^3 . Heat exchange between the table and the substrate holder was maintained by supplying helium at $P = 10$ Torr. RF power was varied from 1 to 20 W with a 2 W step and ICP power was varied from 500 to 2100 W with a 200 W step.

The effect of process parameters on deposited dielectric film parameters was studied for deposition onto silicon substrates. Electrical parameters of transistors for different passivation modes were studied for test HEMT specimens with 1 mm gate length, 8 mm drain-source distance and 100 to 500 mm width. Schematic of a test structure is shown in Fig. 1.

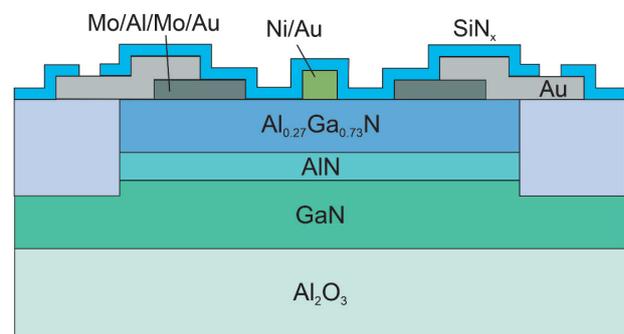


Figure 1. Schematic of test HEMT structure.

The initial substrate was an AlGaN/GaN heterostructure grown on a sapphire Al_2O_3 substrate 75 mm in diameter and 450 mm in thickness. The heterostructure had the following parameters: 16 nm thick $Al_{0.27}Ga_{0.73}N$ barrier layer, 0.7 nm thick intermediate AlN layer and 2.5 nm thick

undoped buffer GaN layer. The layer resistance, electron mobility and layer concentration in 2D electron gas measured by a contactless eddy current method were 245 Ohm/□, 1990 cm²/(V·s) and 1.13 · 10¹³ cm⁻², respectively.

First we fabricated ohmic contacts from Mo/Al/Mo/Au metallization which was formed by electron beam sputtering [21]. The as-sputtered contacts were annealed at 850 °C for 30 s in a nitrogen atmosphere. Before forming Schottky barriers the active regions of the test specimens were isolated by Ar ion implantation on a HVE 100. The Schottky barriers were made from Ni/Au metallization which was also formed by electron beam sputtering [3]. The Schottky barriers were thermally annealed at 350 °C for 10 min in a nitrogen atmosphere. Then to reduce the serial resistance of the deposited contacts we halvanically deposited a 2 mm gold layer (Au).

Immediately before dielectric deposition we removed the oxide layer with a 20% ammonia sulfide etchant solution for 1 min. The films deposited onto the test transistor structures were 200 nm thick.

The silicon nitride films deposited onto the silicon substrates for controlling dielectric parameters were 100 nm thick. The working surfaces of the silicon wafers were prepared for the process by washing in a standard etchant, i.e., an ammonium hydroxide and hydrogen peroxide mixture with NH₄OH : H₂O₂ = 1 : 4 for 3 min with preliminary etchant heating. The wafers were then rinsed in deionized water and compressed air dried.

The film thicknesses and refraction indexes were measured by ellipsometry using a LEM-2M instrument. The test specimen cross-sections were imaged with scanning electron microscopy on a JEOL JSM-6480LV with a sharp-focused ion beam on a FEI-601.

The current vs voltage curves of the test specimens were taken with an Agilent B1500A semiconductor device analyzer and a Cascade Microtech PA200 probe station. The transistor output characteristics were measured up to a 20 V drain-source bias voltage, the gate bias was varied between 0 and -5 V with a 0.5 V step and the maximum current vs voltage curve slope was evaluated at $U_{DS} = 10$ V. The closed gate drain-source leakage (non-cutoff) currents were measured at $U_{DS} = 50$ V.

3. Results and discussion

First we measured the refraction index and growth rate of the dielectric films for different deposition modes (we varied the RF and ICP power and working gas flow ratios). The deposition rate changed but slightly with an increase in the RF power but grew with an increase in the ICP power. For example, at RF = 1 W and ICP = 500 W the growth rate was 0.25 nm/s while at RF = 1 W and ICP = 2100 W it was 0.75 nm/s.

Figure 2 shows film refraction index n as a function of RF and ICP power. It can be seen that the refraction index decreases but little with an increase in the ICP power from 500 to 2100 W and increases with an increase

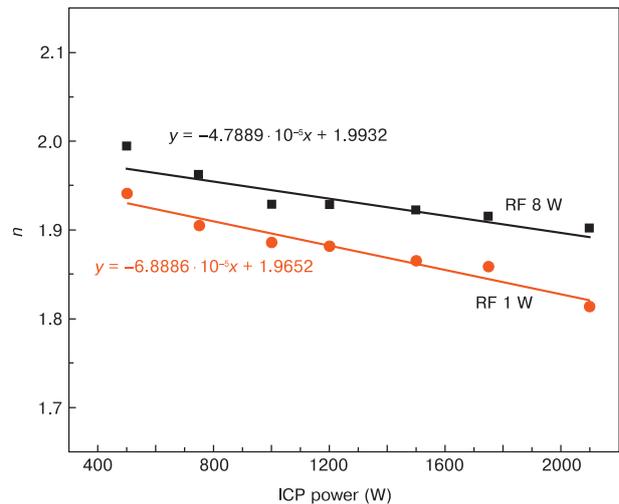


Figure 2. Refraction index n as a function of ICP and RF power.

in the RF power from 1 to 8 W. This refraction index dependence on RF and ICP power can be attributed to change in the dielectric film composition [22, 23]. An increase in the ICP power leads to an increase in the nitrogen content in the film due to a greater dissociation rate of nitrogen molecules in the ICP source, and this provides for a higher refraction index. An increase in the RF power causes a more intense decomposition of monosilane molecules (monosilane is supplied from the “shower” near the substrate), and this increases the refraction index due to an increase in the quantity of silicon incorporated into the film.

Cross-sections of the AlGaIn/GaN heterostructure test specimens passivated with SiN_x silicon nitride were SEM imaged. Figure 3 shows a SEM image of a test specimen cross-section. It can be seen that the deposited dielectric film was 215 ± 10 nm thick and the film thickness on the side surface was 150 ± 10 nm. Thus the deposition was almost conformal.

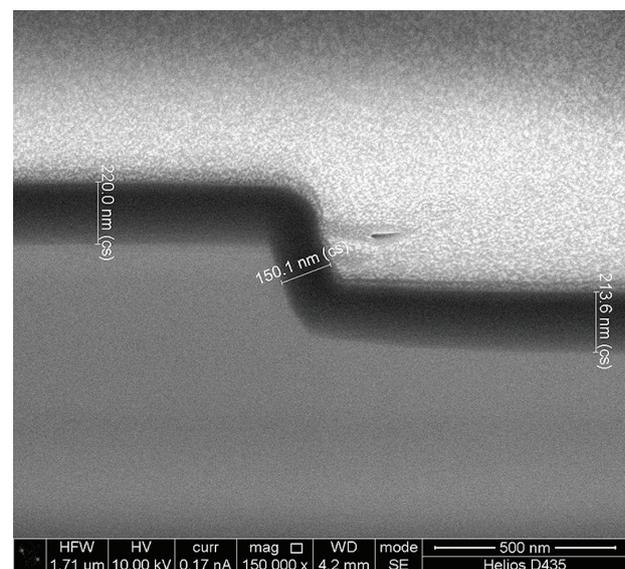


Figure 3. SEM image of test specimen surface.

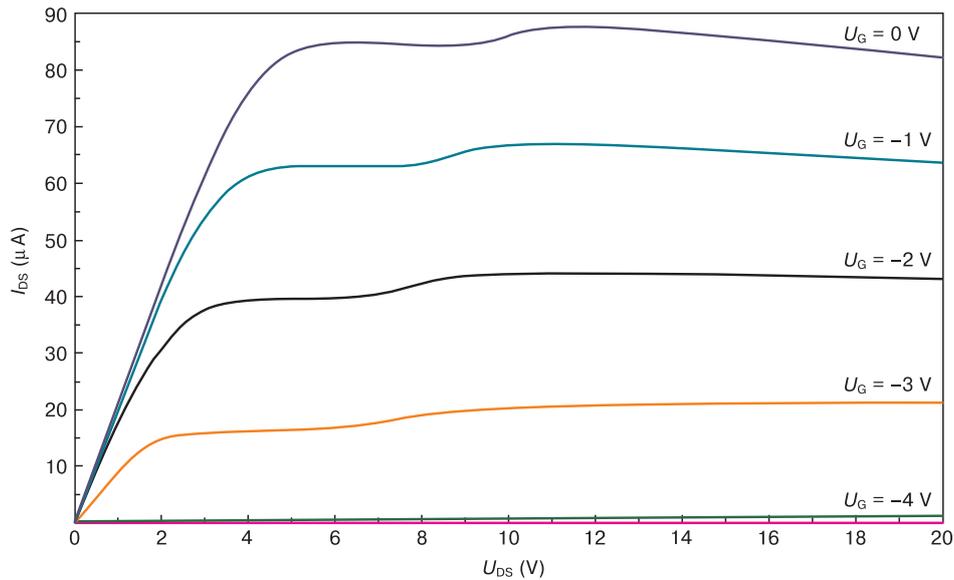


Figure 4. Output current vs voltage curves for 200 mm wide gate AlGaIn/GaN HEMT.

We measured the output current vs voltage curves of the test transistor specimens. Figure 4 shows the output characteristic of the specimen passivated at $P = 10$ mTorr, $T = 100$ °C, RF = 1 W, ICP = 1200 W and $\text{SiH}_4/\text{N}_2 = 13.9/13.1$. The open state saturation current I_{DS} was approx. 90 mA (gate width 200 mm) and zero gate bias current saturation was reached at $U_{\text{DS}} = 4$ V. The test transistor cut off at $U_{\text{G}} = -4.2$ V, the closed state drain–source current was $I_{\text{non-cutoff}} = 1.8$ mA at a 50 V source–drain bias voltage.

Furthermore the above mode yielded the greatest transistor slope $S = 115$ mS/mm. The transistor slope decreased considerably with an increase in the RF power: it was the greatest at minimum power RF = 1 W. This is because an increase in the RF power leads to an increase in the auto bias between the plasma and the table and hence an increase in the ion bombardment energy which causes strong radiation damage to the surface at low pressure (10–100 mTorr). The experiment showed that in the beginning of growth even at a low RF power (3 W) the transistor structure becomes completely inoperable. THUS dielectric deposition for HEMT passivation should be started at minimum RF power.

The AlGaIn/GaN microwave HEMT passivation process developed by us provides for conformal films and low closed transistor drain–source currents without compromise in open state transistor performance, i.e., within 15 and 100 mA, respectively, for a 1.25 and 5 mm common T-gate ($U_{\text{G}} = -8$ V and $U_{\text{DS}} = 50$ V).

4. Conclusion

The ICP CVD method allows depositing conformal SiN_x dielectric films for AlGaIn/GaN HEMT passivation.

We selected and developed a basic HEMT passivation process with the following parameters: $P = 10$ mTorr, $T = 100$ °C, RF = 1 W, ICP = 1200 W and $\text{SiH}_4/\text{N}_2 = 13.9/13.1$. This dielectric deposition mode provided for lowest closed state currents and greatest output current vs voltage curve slope of the test AlGaIn/GaN HEMT specimen.

This passivation mode provides for low currents in closed high-power microwave HEMT without compromise in open state transistor performance.

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