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Research Article

Use of atomic force microscope for the synthesis of GaAs/AlGaAs heterostructure base one-dimensional structure

Mikhail V. Stepushkin[1], Vladimir G. Kostishin[2], Vladimir E. Sizov[1], Alexei G. Temiryazev[1]

1 Kotelnikov Institute of Radioengineering and Electronics of RAS (Fryazino Branch), 1 Vvedensky Sq., Fryazino, Moscow Region 141190, Russia
2 National University of Science and Technology MISiS, 4 Leninsky Prospekt, Moscow 119049, Russia

Corresponding author: *Mikhail V. Stepushkin* (cokpoweheu@yandex.ru)

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Abstract

Electron transport in low-dimensional structures is often studied using semiconductor heterostructures with two-dimensional electron gas in which insulating regions separating the conducting channel from the gates are synthesized using one of available methods. These structures are distinguished by the high quality of the initial wafers and the necessity to change the surface topology during the study, this making photolithography ineffective.

In this work we analyze the technology of insulating grooves that uses atomic force microscope, i.e. the pulse force nanolithography, which allows either treating single samples or forming narrow and deep grooves on semiconductor surfaces to provide good insulation. The experimentally measured transport characteristics of the nanostructures produced using this method confirm channel conductance quantization and the absence of large quantities of introduced defects.

Keywords

GaAs/AlGaAs heterostructre, atomic force microscope, two-dimensional electron gas, nanostructure, pulse force nanolithography, local anodic oxidation method, channel conductance quantization

1. Introduction

The synthesis and study of one-dimensional and zero-dimensional nanostructures is a rapidly developing trend of theoretical and experimental solid state physics since as the dimensions of active semiconductor elements approach the nanometer range the quantum properties of electrons become increasingly expressed. This on the one hand impairs the performance of the classic elements which are based on electron's behavior as a particle while on the other hand shows good promise for the development of new active elements for data processing systems based on quantum-size effects.

Nanostructure samples are used for the experimental study of carrier transport in nanostructures. Nanostructure sample synthesis methods are multiple, e.g. growth of nanowires [1] or metallic films [2], MOS structure formation etc. but the most universal technique is the growth of selectively doped semiconductor hererostructures such as GaAs/$Al_xGa_{1-x}As$ (see e.g. [3, 4]), in which a two-di-

mensional electron gas **(2DEG)** layer with a high electron mobility forms at the heterointerface. When nanostructures are formed the electron transport in the 2DEG plane is restricted by potential barriers which are typically produced using the following methods. The split gate method implies producing two metallic electrodes on the semiconductor structure surface which are then negatively biased for forming depletion regions that limit the conducting channel in the semiconductor [5]. For the in plane gate method, insulating regions are produced in the semiconductor that limit the 2DEG regions acting as the channel and the gates. Synthesis of the gates in the 2DEG layer reduces their screening of the electron-electron interaction in the channel and hence the charge accumulation in the quantum conductor and the carrier spin polarization caused by the electron-electron interaction.

One condition for quantization is the absence of electron scattering in the channel, i.e., the channel length must be less than the electron path length which is several microns in typical structures at operation temperature (~4.2 K). However under specific conditions quantization may occur at up to 50 K [6]. Important parameters are the insulating region width, depth and breakdown parameters. The synthesis of these structures requires lithography tools with typical element dimensions of ~ 0.1 μm. This is achievable for conventional high-resolution optical or electron lithography processes followed by etching (chemical, ion plasma, plasmochemical) of the grooves as demonstrated earlier [6–8]. These methods are widely used in the batch fabrication of semiconductor devices but their main distinctive feature – batch processing of crystals on the wafer – proves to be unsuitable for laboratory practice due to the need to change the surface topology during analysis and to use extremely high quality initial wafers. An interesting method was developed [9] for drawing insulating regions with a 100 nm diam. focused ion beam that allows synthesizing nanostructures on separate crystal; this method however did not find general use presumably due to the large quantity of introduced defects.

Scanning probe microscope **(SPM)** technologies have recently become increasingly widespread [10]. For example local anodic oxidation **(LAO)** is widely used for the production of insulating regions in nanostructures, this method being based on the electrochemical oxidation of the semiconductor surface as a result of its interaction with adsorbed water films under a negative bias supplied to the SPM conducting probe [11–14]. This method allows applying lithography process for separate packaged sample and does not introduce large quantities of defects. However using LAO for structures with 2DEG depths of greater than 50 nm proved to be inefficient since the insufficiently high breakdown voltage between the gates and the channel did not provide for efficient channel conductance control. Increasing the oxidation depth by applying higher voltage between the microscope probe and the semiconductor led to an increase in the insulating region width thus reducing the channel control efficiency of the gates. Other researchers [15] reported the possibility of using pulsed voltage thus making it possible to process structures with up to 80 nm 2DEG depths.

Another standard surface processing method relying upon atomic force microscopy is surface scratching with a pressed tilted needle. A steel cantilever with a diamond pyramid or a silicon probe with a diamond-like coating is typically used for hard materials. In both variants the tips have a sufficiently large curvature radius (30–50 nm) reducing the space resolution of the lithography process used.

The novel pulse force nanolithography **(PFNL)** method was proposed [17, 18] that allows mechanical processing of hard materials with extremely thin and sharp single crystal diamond needles (tip curvature radius of about 10 nm). Operating such tools implies designing special lithography techniques. A sharp diamond needle can penetrate deeply into almost any material if force is applied along the needle axis; however, the lateral shift of the needle under load may damage it. Scratching surfaces with such tools is inefficient. The method proposed is based on fast pointwise indentation (pinning) with small (5–20 nm) point spacing. An important advantage of this method is the possibility of providing grooves with the depth-to-width ratio R of more than 1 unlike R = 0.1–0.3 typical of LAO.

2. Experimental

The test samples were fabricated from GaAs/AlGaAs heterostructures grown by molecular beam epitaxy **(MBE)** on semiinsulating GaAs substrates. The layer growth sequence was 1 μm undoped GaAs, 100 nm AlGaAs and 35 nm protective undoped GaAs. The AlGaAs layer contained two Si doped delta layers. The spacer thickness (the distance from the heterointerface where 2D electron gas forms in the triangular potential well of GaAs, to the nearest delta layer) was 50 nm. The 4.2 K electron concentration and mobility in the 2D layer were 3.5×10^{11} cm^{-2} and 3.5×10^5 $cm^2/(V \times s)$, respectively, the electron free path being 3–5 μm.

At the first stage which is similar to the earlier described one [14, 16] a ~150 nm high mesostructure was formed on the heterostructure surface with standard optical lithography and chemical etching. Then the Ni/Ge/Au system [19–21] of Ohmic contacts to the drain, source and gate regions was formed by lift-off lithography. Further grooves were formed using optical lithography and chemical etching for separating hetestructure regions where groove width was not critical. Following that the structures were packaged in the housing of the chip.

At the second stage nanostructures were synthesized in each sample using PFNL with a Smart SPM, AIST-NT7.

The PFNL operation principle can be demonstrated for the following example of forming four grooves in a semiconductor using different numbers of passes. Initially multiple indentations are sequentially made at 1 nm spacing with a 50 nm vertical amplitude (the vertical amplitude measu-

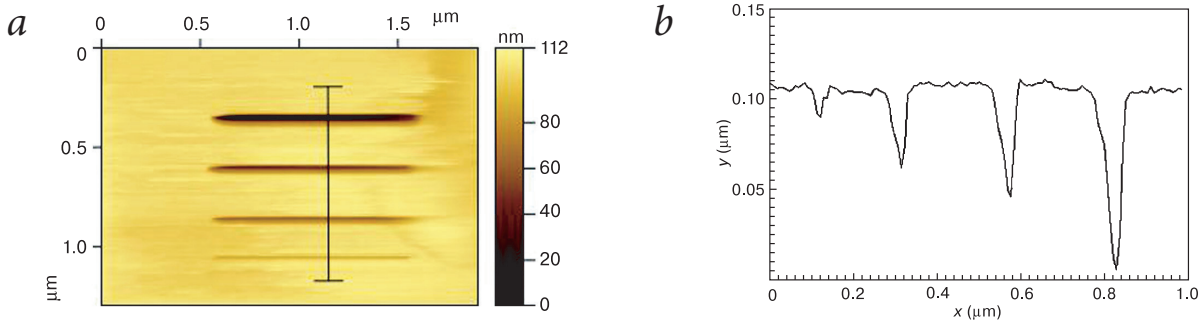

Figure 1. (*a*) SPM image and (*b*) surface profile along the marked line of sample with several grooves formed using (upward) 1, 20, 30 and 100 needle passes.

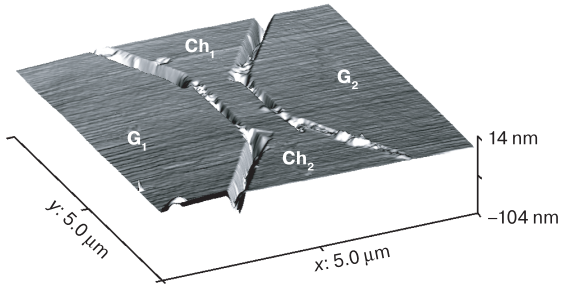

Figure 2. SPM image of nanostructure with two G_1 and G_2 controlling side gates and Ch_1–Ch_2 channel.

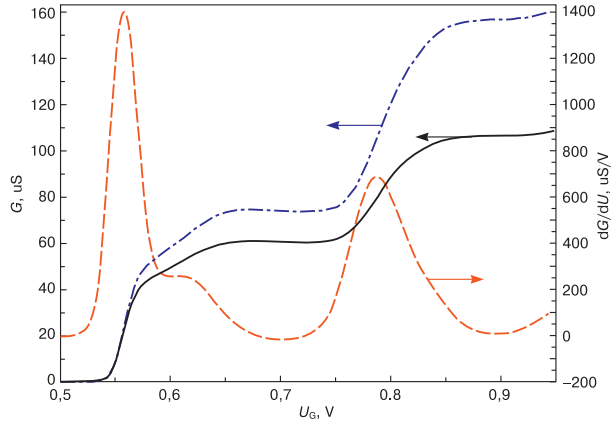

Figure 3. Sample conductance G (solid curve), channel conductance without allowance for contact resistance (dot-and-dash curve) and dG/dU derivative (dashed curve)) as a function of gate voltage U_G, used for more accurate quantization step positioning.

rement did not take into account the cantilever elasticity, so the actual needle penetration depth into the semiconductor was less, about 20 nm). One can make more indentation passes to obtain deeper grooves. Fig. 1 *a* shows SPM images of grooves for 1, 20, 30 and 100 passes. As can be seen from the depth profile shown in Fig. 1 *b* the groove depth after 100 passes is about 100 nm, the width being about 35 nm, i.e., the depth to width ratio R is about 3.

Thus a nanostructure consisting of a channel and two gates was formed. Fig. 2 shows its SPM image. Same as for conventional field transistors the electrostatic field of the gates controls the channel conductance.

The electrical parameters of the structures were measured at 1.5–4.2 K. For the measurements the samples were placed in a vacuum attachment submerged into a transport liquid helium Dewar flask. The DC CV curves of the gates showed that the leakage currents were within 1 nA even at >1 V voltages.

The differential conductance (G) of the channel as a function of the gate voltage (U_G) was measured at DC with the lock-in detection method. The solid curve in Fig. 3 shows one of the differential conductance curves taken at 1.5 K. It shows well the conductance quantization steps and the "0.7 feature" which suggests [4] a high structural quality. The mismatch between the experimental absolute values of the conductance steps and the theoretical ones are due to the contact and conductor resistances which totaled to about 3 kOhm in our experiment. Having subtracted the contribution of these resistances we obtained the dependence shown in Fig. 3 with the dot-and-dash curve. The step conductances are G = 75 and 156 μS, i.e., close to the theoretical values G_0 = 77.5 and $2G_0$ = 155 μS. Furthermore, for more accurate step positioning Fig. 3 (dashed curve) shows the dG/dU_G derivative as a function of gate voltage. The clearly expressed channel conductance quantization confirms that electron transport in the channel is ballistic, i.e., PFNL does not introduce any significant quantity of defects into the semiconductor lattice.

3. Conclusion

The results suggest that PFNL can be successfully used in laboratory practice for producing insulating grooves in AlGaAs/GaAs heterostructures with 2D electron gas. Like all atomic force microscope based methods it allows using lithography processes for separate packaged crystal with quick topology change option during analysis. The method allows producing grooves with depth to width ratios of more than 1, also in structures with deep (more than 50 nm) 2D electron gas localization. The breakdown voltages of such grooves may reach several Volts at leakage currents of less than 1 nA.

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