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Short Communication

Passivation of substrates with hydrogen to reduce the number of electron traps in the buffer layer at the contact of silicon with $Ba_{1-x}Sr_xTiO_3$

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Abstract

The performance of FeRAM non-volatile cells including those on ferroelectric insulating layers requires full-scale development of the field effect at the semiconductor–dielectric interface. The recharging of electron traps concentrated in the buffer layer between the insulator and the wafer impedes the development of the field effect at the interface. A Si wafer has been hydrogen-saturated for suppressing the activity of electron traps in the buffer layer at the ferroelectric–silicon contact. The reference specimen has been another similar wafer not exposed to H_2. High-frequency C–V curves of the metal–dielectric–semiconductor structures with $Ba_{0.8}Sr_{0.2}TiO_3$ insulating layers deposited on both wafers have been measured. The capacities of the test specimens have proven to be low sensitive to hydrogen saturation of the wafers. This is accounted for by long-term heating of the silicon wafers at 500–600 °C during ferroelectric deposition. It has been proposed to implant large organic cations into the wafers in order to reduce the concentration of electron traps in the $Ba_{0.8}Sr_{0.2}TiO_3$–Si buffer layers. Those organic cations can be 2–phenylethyl ammonium iodide, 4-chlorophenylethyl ammonium iodide and 4-fluorophenylethyl ammonium iodide which showed good results at passivation of high-performance metal–halogenide perovskite solar cells.

Keywords

silicon–ferroelectric contact buffer layers, dangling bond passivation, high-frequency C–V curves

1. Introduction

Electronics engineering will soon change for ICs with insulating layers of various materials, e.g. high-k dielectrics and ferroelectrics deposited onto silicon wafers. The large lattice mismatch between the deposited dielectric and the semiconductor causes the formation of the so-called buffer layer at their contact [1] mainly containing oxides of the contacting materials. Although that layer is typically far thinner than the insulating gap, it plays a significant role during structure recharging by impeding the development of the field effect including the opening of

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minority carrier channels [2, 3]. The latter exerts a highly deleterious impact on the performance of devices, including FeRAM non-volatile memory cells in which information reading is based on measuring the sub-gate channel conductivity at the depleted semiconductor surface. This buffer layer behavior is attributed to the high concentration of dangling silicon and deposited metal bonds. Those dangling bonds act as electron traps the recharging of which screens the penetration of external electric fields into the wafer.

Electron trap hydrogen passivation is used for suppressing the activity of surface electron localization centers in an advanced planar silicon technology [4, 5]. It is therefore reasonable to test that approach for structures containing ferroelectric insulating layers. One should however bear in mind that annealing of silicon–ferroelectric–metal specimens in a molecular hydrogen saturated atmosphere significantly reduces the random polarization of the objects [6–8]. Therefore hydrogen saturation should be applied to the wafer specially prepared for insulating layer deposition rather than to the whole specimen. The latter approach is described in this work. Below we will describe the procedure of silicon wafer exposure to hydrogen containing media, preparation of metal–dielectric–semiconductor (MDS) structures and data on high-frequency C–V measurements for passivated and non-passivated wafers.

2. Experimental

The test wafers were 460 mm thick *p*-type conductivity KDB-10 silicon wafers. The doping impurity concentration as calculated from the resistivity was $N_A \approx 1.25 \cdot 10^{15}$ cm^{-3}. One of the two similar silicon wafers was hydrogen-saturated in a commercial solar cell fabrication line, whereas the other was not exposed to H_2 but used as a reference for comparing the results. 300 nm thick $Ba_{0.8}Sr_{0.2}TiO_3$ (BST) layers were synthesized on each wafer by high-frequency polycrystalline target sputtering in an oxygen atmosphere. Then 100 nm thick nickel electrodes with the areas $S \approx 2.7 \cdot 10^{-4}$ cm^2 were deposited onto the BST surface through a shadow mask by electron beam evaporation. A more detailed description of the plant design and deposition techniques is available elsewhere [9, 10].

The impedance of the test specimens was measured at room temperature at 1 MHz with a V_g = 200 mV/s field voltage sweep rate on a LCR Agilent E4980A precision meter. For a detailed description of the experimental setup see [11].

3. Results and discussion

The C–V curves of the structures grown on hydrogen-exposed and reference wafers are shown in Fig. 1. Comparison between Fig. 1*a* and Fig. 1*b* showed that silicon wafer exposure to a hydrogen-saturated media did not fundamentally suppress the activity of electron traps concentrated in the buffer layer between the ferroelectric and the semiconductor. The structures grown on the hydrogen-passivated wafer had a slightly greater difference between the high-frequency capacities on the C–V curve plateau, i.e., 76 and 9.5 pF against 61.8 and 7.2 pF for the non-H_2-passivated specimens. However, the maximum capacities in both cases are far lower than the 1 MHz capacity of the metal–dielectric–metal structure with insulating BST layer of the same thickness as in the test specimens. Thus, as follows from earlier data [2, 12], both types of test structures exhibit strong screening of external electric fields during recharging of the electron traps concentrated in the BST–silicon contact buffer layer. The decrease in the measured capacity with an increase in voltage agrees with the slight band bending in the semiconductor. The capacity of silicon for flat bands C_{sfb} is written as

$$C_{sfb} = S\left(\frac{\varepsilon_s q^2 N_A}{4T\pi}\right)^{1/2},$$

where q is the unit charge, T is the absolute temperature in energy units and ε_s is the dielectric permeability of Si.

For the calculated N_A and room temperature, C_{sfb} is 24.15 pF. The dependence of semiconductor capacity C_s on external bias V_s is described as follows

$$C_s = C_{sfb}\frac{\left|1-e^{-v_s}\right|}{2^{1/2}\left\{v_s + e^{-v_s} - 1\right\}^{1/2}}, \quad (1)$$

where $v_s = qV_s/T$ is the dimensionless band bending in silicon which is $v_s > 0$ for a depleted state and $v_s < 0$ for an enriched state. Therefore in accordance with Eq. (1), it follows from Fig. 1 that the dimensionless band bending in the semiconductor varies from –2.9 to 4.2 in the hydrogen-passivated wafer and from –2.1 to 6.5 in the reference one. Thus, Si wafer exposure to H_2 resulted in a slight narrowing (by $2T$ in energy units) of the minimum of the U-shaped spectral energy curve for the electron traps in the buffer layer of the MDS structure and its slight shift towards the silicon valence band top.

The low sensitivity of the test MDS structures to hydrogen saturation of the wafers is most likely due to the temperature conditions of BST deposition onto the silicon wafer. The conditions T = 500–650 °C are maintained during polycrystalline target sputtering in a Plazma-50SE plant (Russia) for a long time, about one hour. Therefore the protons trapped by the dangling silicon bonds have time to activate and hydrogen can evaporate from the wafer to the atmosphere. It should be noted that for an advanced thermal oxidation planar silicon technology (radical thermal oxidation with in situ steam generation, ISSG) [14], high hydrogen concentration is maintained in the reaction zone throughout the entire process which leads to successful electron trap passivation. The main

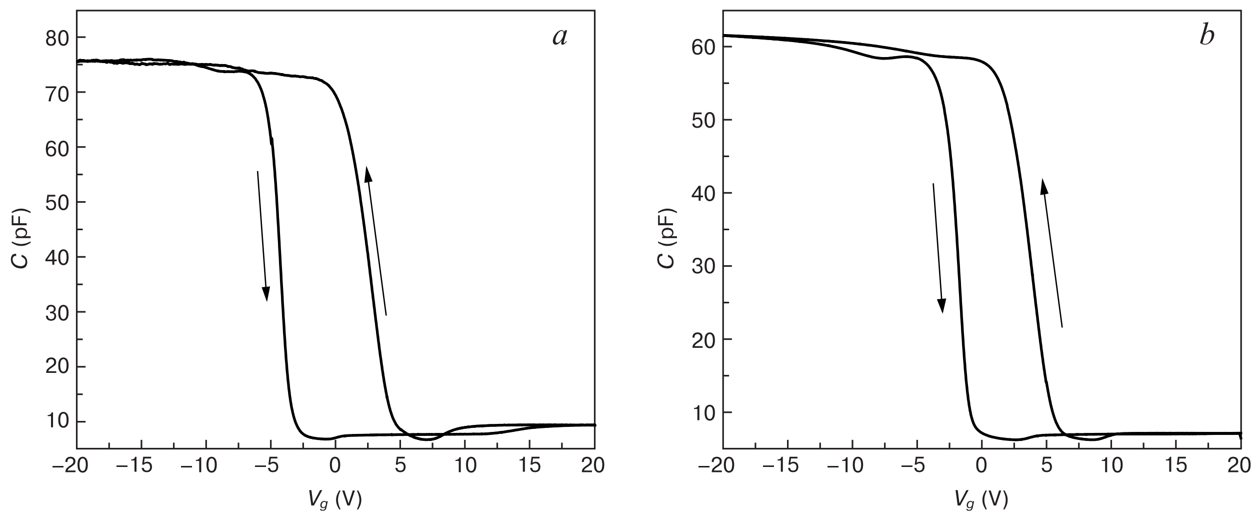

Figure 1. High-frequency C–V curves of the MDS structures on (*a*) hydrogen-passivated wafer and (*b*) reference wafer: *C* is specimen capacity and V_g is field voltage

conclusion from this work is that for MDS structures in which the deposition of insulating layers requires high-temperature conditions or annealing, hydrogen exposure of silicon wafers for electron trap passivation in the buffer layer is useless. Here one should mention the good passivation results for high-performance metal–halogenide perovskite solar cells delivered by implantation of large organic cations, e.g. 2-phenylethyl ammonium iodide, 4-chlorophenylethyl ammonium iodide and 4-fluorophenylethyl ammonium iodide [15]. The latter approach does not change the bulk crystalline structure of perovskite and leads to efficient passivation of defects at its boundaries.

4. Conclusion

The studies of electrical activity reduction of surface electron traps at BST–Si contacts should be driven by the use of passivating materials with heavy cations or anions that are stable at up to 600 °C and do not evaporate from the wafers during heating in MDS deposition processes. One should obviously not restrict oneself to the above-mentioned chloro-, fluoro- and phenylethyl ammonium iodides [15]. In this context, it would be appropriate to mention experiments for silicon surface passivation with 1-octadecene organic monolayers [16]. The general criterion of electron trap passivation in the BST–Si buffer layer is an abrupt decrease in the concentration of the recharging localized electron states and a weak effect on the bulk crystalline structure of the ferroelectric deposited onto silicon.

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References

1. Park J.Y., Yang K., Lee D.H., Kim S.H., Lee Y., Reddy P.R.S, Jones J.L., Park M.H. A perspective on semiconductor devices based on fluorite-structured ferroelectrics from the materials–device integration perspective. *Journal of Applied Physics*. 2020; 128: 240904. https://doi.org/10.1063/5.0035542
2. Goldman E.I., Chucheva G.V., Belorusov D.A. On the form of high-frequency voltage-capacitance characteristics of metal-insulator-semiconductor structures with a ferroelectric insulating layer $Ba_xSr_{1-x}TiO_3$. *Ceramics International*. 2021; 47(15): 21248–21252. http://dx.doi.org/10.1016/j.ceramint.2021.04.129
3. Belorusov D.A., Goldman E.I., Chucheva G.V. A weak manifestation of the field effect in metal-dielectric-semiconductor structures with a ferroelectric insulating layer $Ba_{1-x}Sr_xTiO_3$. *Physics of the Solid State*. 2022; 64(13): 2140–2142. http://dx.doi.org/10.21883/FTT.2021.11.51592.154
4. Poindexter E.H. MOS interface states: overview and physicochemical perspective. *Semiconductor Science and Technology.* 1989; 4(12): 961–969. https://doi.org/10.1088/0268-1242/4/12/001
5. Bonilla R.S., Hoex B., Hamer P., Wilshaw P.R. Dielectric surface passivation for silicon solar cells: A review. *Physica Status Solidi A.* 2017; 214(7): 1700293. https://doi.org/10.1002/pssa.201700293
6. Aggarwal S., Perusse S.R., Tipton C.W., Ramesh R. Effect of hydrogen on Pb(Zr,Ti)O_3-based ferroelectric capacitors. *Applied Physics Letters.* 1998; 73(14): 1973–1975. https://doi.org/10.1063/1.122339
7. Im J., Auciello O., Krauss A.R., Gruen D.M., Chang R.P.H., Kim S.H., Kingon A.I. Studies of hydrogen-induced degradation processes in

$SrBi_2Ta_2O_9$ ferroelectric film-based capacitors. *Applied Physics Letters.* 1999; 74(8): 1162–1164. https://doi.org/10.1063/1.123474

8. Shimakawa Y., Kubo Y. Degradation of ferroelectric $SrBi_2Ta_2O_9$ materials under reducing conditions and their reaction with Pt electrodes. *Applied Physics Letters.* 1999; 75(18): 2839–2841. https://doi.org/10.1063/1.125167
9. Ivanov M.S., Afanasyev M.S. Features of the formation of thin ferroelectric $Ba_xSr_{1-x}TiO_3$ films on various substrates by high-frequency sputtering. *Fizika tverdogo tela.* 2009; 51(7): 1259–1262. (In Russ.)
10. Kiselev D.A., Afanasyev M.S., Levashov S.A., Chucheva G.V. Kinetics of induced domain growth in ferroelectric thin films $Ba_{0.8}Sr_{0.2}TiO_3$. *Fizika tverdogo tela.* 2015; 57(6): 1134–1137. (In Russ.)
11. Gol'dman E.I., Zhdan A.G., Chucheva G.V. Determination of the coefficients of ion transfer in insulating layers on the surface of semiconductors using dynamic current-voltage depolarization characteristics. *Instruments and Experimental Techniques* . 1997; 40(6): 841–846.
12. Goldman E.I., Chucheva G.V., Belorusov D.A. The role of a buffer layer at the contact with silicon in structures with an insulating gap made of a material replacing SiO_2. *Ceramics International.* 2024; 50(6): 9678–9681. http://dx.doi.org/10.1016/j.ceramint.2023.12.286
13. Zi S. Physics of semiconductor devices. Moscow: ITS Media; 2024. 656 p. (In Russ.)
14. Chernyaev M.V., Gorokhov S.A., Rezvanov A.A., Patyukov S.I. Kinetics of radical oxidation of silicon. *Electronic engineering. Series 3. Microelectronics.* 2022; (3(187)): 31–45. (In Russ.). https://doi.org/10.7868/S2410993222030058
15. Jiang Q., Ni Zh., Xu G., Lin Y., Rudd P.N., Xue R., Yun L. Interfacial molecular doping of metal halide perovskites for highly efficient solar cells. *Advanced Materials.* 2020; 32: 2001581. http://dx.doi.org/10.1002/adma.202001581
16. Antonova I.V., Soots R.A., Seleznev V.A., Prince V.Ya. Electrical passivation of the silicon surface by organic monolayers of 1-octadecene. Semiconductors. 2007; 41: 991–997. https://doi.org/10.1134/S1063782607080246