MOEM

Modern Electronic Materials 2022; 8(3): 107–111
DOI 10.3897/j.moem.8.3.98145

Research Article

Simulation of time to failure of porous dielectric in advanced topology integrated circuit metallization system

Andrey A. Orlov[1,2], Askar A. Rezvanov[1,2]

1 *Molecular Electronics Research Institute, JSC, 6-1 Acad. Valieva Str., Zelenograd, Moscow 124460, Russian Federation*
2 *Moscow Institute of Physics and Technology (National Research University), 9 Institutskiy Lane, Dolgoprudny, Moscow Region 141701, Russian Federation*

Corresponding author: Andrey A. Orlov (aorlov@niime.ru)

Received 12 November 2021 ♦ **Accepted** 28 December 2021 ♦ **Published** 20 October 2022

Citation: Orlov AA, Rezvanov AA (2022) Simulation of time to failure of porous dielectric in advanced topology integrated circuit metallization system. *Modern Electronic Materials* 8(3): 107–111. https://doi.org/10.3897/j.moem.8.3.98145

Abstract

In this work, the simulation of the processes of diffusion of metal barrier ions into a low-k dielectric between two nearby copper lines was performed. Based on experimental data on the diffusion coefficient published in the scientific literature and calculations according to the mathematical model of the distribution of metal barrier ions in the dielectric, the time dependent breakdown of a porous low-k dielectric in the elements of very large-scale integrated circuits of the modern topological level was estimated. Additionally, the work obtained dependences of the dielectric breakdown time on the distance between two nearby copper lines along with dependence on the power voltage of the line (the other line is grounded).

Keywords

low-k dielectric, porosity, time dependent dielectric breakdown, copper metallization

1. Introduction

With the permanent reduction of topological level in the fabrication of very large scale integrated circuits **(VLSI)** and the introduction of new materials (e.g. porous low-k SiOC dielectrics) under the International Roadmap for Devices and Systems (IRDS 2020), the time dependent dielectric breakdown **(TDDB)** is among the main problems causing VLSI failure [1]. Time dependent dielectric breakdown is a mechanism of failure in the metallization system when dielectric breakdown results from a long-term exposure to an electric field.

The main causes of VLSI degradation in copper metallization systems for ≤90 nm topological level are copper ion diffusion and drift into the dielectric under an external electric field [2–5]. However, ≤32 nm design topological level require potential ion currents in the diffusion barrier between the copper and the dielectric be taken into account.

The cause of TDDB is believed to be the formation of a conducting layer of traps connecting two nearby metallization lines (electrodes) which eventually leads to a significant current increase. It is believed that the traps (localization centers of electrons tunneling from electrodes)

© 2022 National University of Science and Technology MISiS. This is an open access article distributed under the terms of the Creative Commons Attribution License (CC-BY 4.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original author and source are credited.

are formed by diffusion of metallic barrier ions (e.g. Ta/TaN) [6]. The local conductivity between copper lines depends on the probability of an electron jump between nearby centers which in turn is an exponential function of the distance between the centers (Eq. (1)):

$$\sigma_{i,j} \sim \gamma^0_{i,j} \exp\left\{-\frac{2r_{i,j}}{a} - \frac{\varepsilon_{i,j}}{k_B T}\right\}. \qquad (1)$$

where $r_{i,j}$ is the distance between the i and j centers, a is the radius of electron localization at these centers, $\varepsilon_{i,j}$ is the energy barrier between the two centers, k_B is Boltzmann's constant and T is the temperature.

The traps form a network of resistors where the resistivity $R_{i,j}$ between the i and j centers is inversely proportional to the local conductivity $\sigma_{i,j}$. Furthermore, the distance $r_{i,j}$ in the 2D system is determined by the concentration of the metallic barrier ions $C(x,y,t)$ which for the considered layer is expressed as $r_{i,j} = C(x,y,t)^{-1/2}$ [7]. Due to the difference in the distance between the centers and the exponential difference between the resistivities, the full resistance of the conducting path is determined by the minimum value of the concentration (schematic in Fig. 1; d is the distance between the copper lines).

The aim of this work is to develop a mathematical model of the distribution of metal barrier ions in a low-k dielectric and to estimate the influence of the input

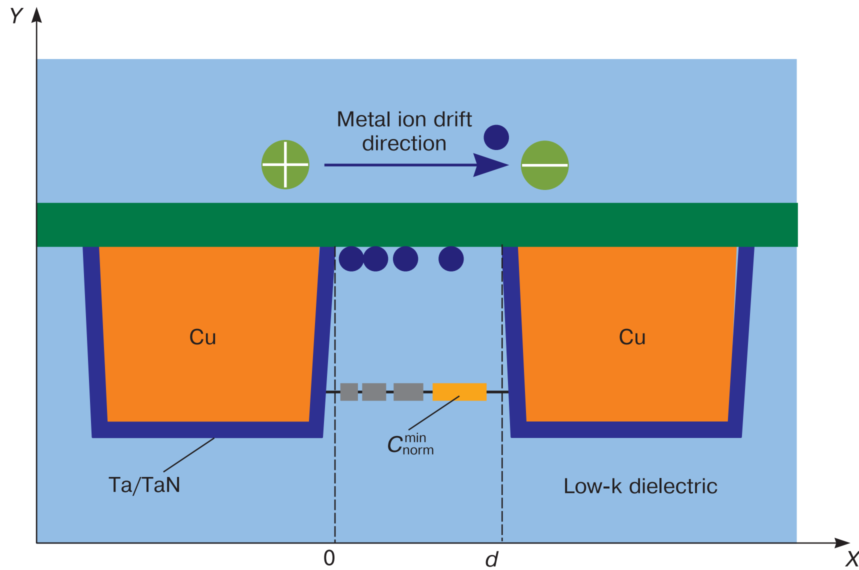

Figure 1. Schematic of physical processes in simulated structure containing two nearby copper lines separated by dielectric [9]. Input parameters: T is temperature, D is metal atom diffusion coefficient in dielectric, k is dielectric permeability of dielectric and E is electric field magnitude between copper lines

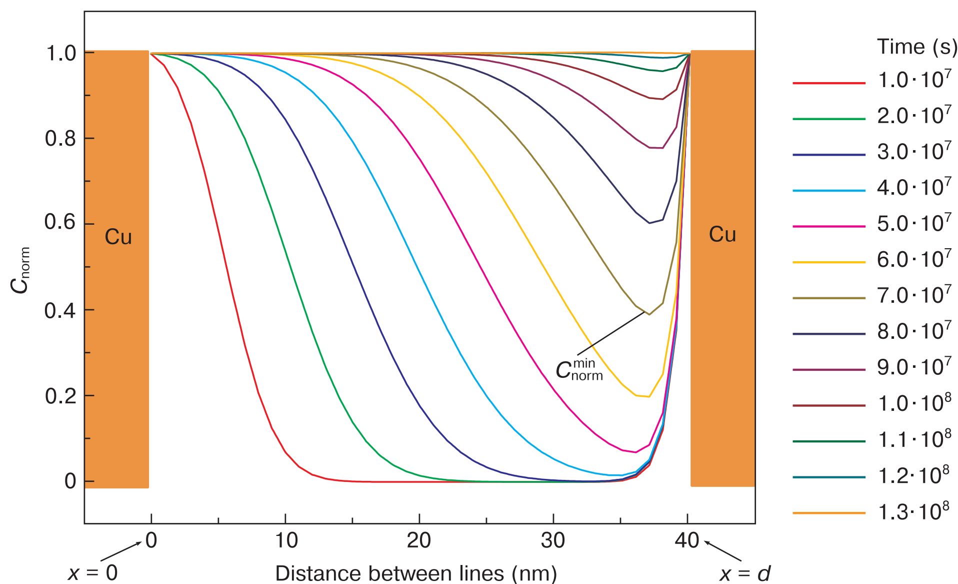

Figure 2. Distribution of ion concentration in metallic barrier between two nearby copper lines. Input parameters: $k = 2.9$; $d = 40$ nm; potential difference $\Delta V = 1.1$ V; $D = D_0 \exp(-E_a/k_B T)$, where $D_0 = 2 \cdot 10^{-11}$ m²/s, activation energy $E_a = 0.9$ eV and $T = 333$ K

parameters of the model on the numerical value of the time dependent breakdown of the dielectric.

2. Simulation of time dependent dielectric breakdown

The normalized minimum concentration of the metal ions $C_{\text{norm}}^{\text{min}}$ can be determined from the equation of diffusion and ion drift in electric field (Eq. (2)) and the boundary conditions at the electrodes (Eq. 3)) [8]:

$$\frac{\partial C_{\text{norm}}}{\partial t} = D\Delta C_{\text{norm}} - qDE\frac{\nabla C_{\text{norm}}}{k_{\text{B}}T}; \quad (2)$$

$$C_{\text{norm}}\,(x=0) = C_{\text{norm}}\,(x=d) = 1. \quad (3)$$

The calculations of the normalized metallic ion concentration between two nearby copper lines as a function of time as illustrated in Fig. 2 were carried out using Multiphysics® COMSOL software by the finite elements methods (the input parameters of simulation are shown on the top of Fig. 2) [7]. The normalized concentration *vs* time $C_{\text{norm}}^{\text{min}}(t)$ graph allows to determine the time to failure **(TTF)** of the dielectric under the condition $C_{\text{norm}}^{\text{min}} \approx 1$ (the TTF definition range is shown in Fig. 3). In this considered the TTF is approx. $1.25 \cdot 10^8$ s (≈3.96 years). Similar calculations were also carried out for earlier reported parameters [10]. The TTF obtained for this case is approx. 4 h (the input data are shown in Fig. 4).

The required input parameters for simulation can be obtained from experimental data. It was shown [11] that the average diffusion length of ions can be approximated by the expression $2(Dt)^{1/2}$, where D and t are the ion diffusion coefficient in the material and the diffusion time, respectively. Further, approximating Arrhenius' graph (diffusion coefficient D as a function of temperature T), the parameter D_0 and the diffusion activation energy E_a can be derived from Eq. (4) using the following well-known relationship between the diffusion coefficient and temperature:

$$D = D_0\exp(-E_a/k_BT). \quad (4)$$

Diffusion length can be measured, for example, using transmission microscopy. Also, Arrhenius' graph can be calculated from X-ray diffraction profiles [11].

Figure 5 shows the TTF as a function of the distance d between two nearby copper lines at constant diffusion coefficient D, temperature T and dielectric permeability k.

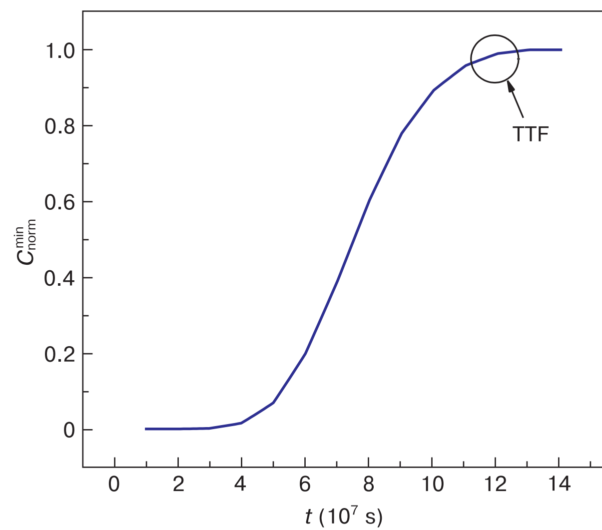

Figure 3. Determination of time to failure (TTF) of porous dielectric

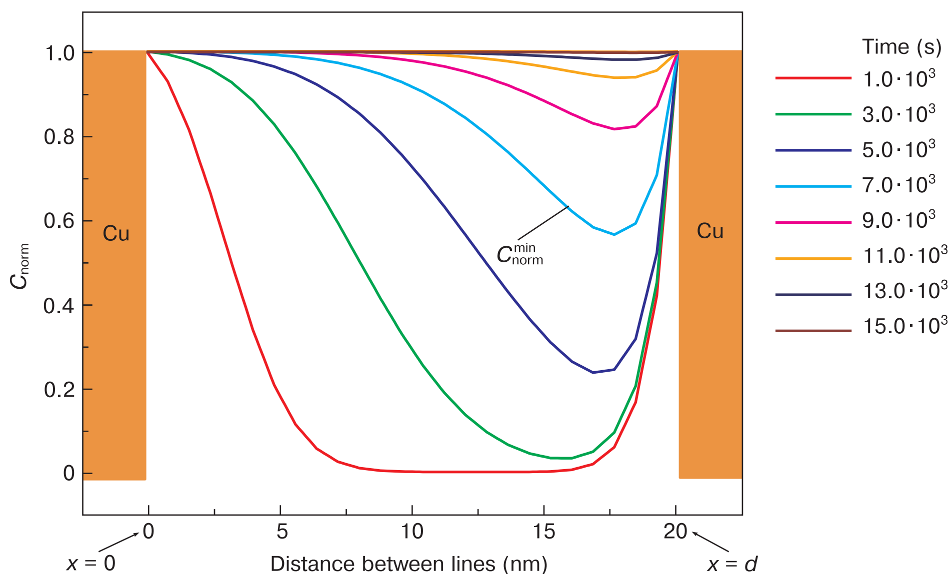

Figure 4. Distribution of ion concentration in metallic barrier between two nearby copper lines. Input parameters: $k = 2.3$; $d = 20$ nm; potential difference $\Delta V = 1.1$ V; $D = 5.1 \cdot 10^{-20}$ m²/s; $T = 673$ K

Approximation of the resultant function has an exponential pattern and is described by the following expression:

$$\mathrm{TTF} = A_1 \exp\left(\frac{d}{t_1}\right) + A_2 \exp\left(\frac{d}{t_2}\right) + \mathrm{TTF}_0. \quad (5)$$

For the parameters used for the simulation in Fig. 2 [7], the coefficients in Eq. (5) are as follows: $A_1 = 3.33739$, $A_2 = 3.33739$, $t_1 = 55.8961$, $t_2 = 68.31746$, and $\mathrm{TTF}_0 = -8.66352$.

In this work the potential difference (or, equivalently, the electric field) between two nearby lines is accepted to be constant which is the case for the following bias line powering schemes: powered line / grounded line, powered line / periodic signal, periodic signal / periodic signal. The case “powered line / periodic signal” will be analyzed in further studies.

Figure 6 shows the TTF as a function of the power voltage V_{DD} (the other line being grounded) at constant diffusion coefficient D, temperature T and dielectric permeability k.

Approximation of the resultant function also has an exponential pattern and is described by the following expression:

$$\mathrm{TTF} = A_1 \exp\left(\frac{V_{DD}}{t_1}\right) + \mathrm{TTF}_0. \quad (6)$$

For the parameters used for the simulation in Fig. 2 [7], the coefficients in Eq. (6) are as follows: $A_1 = 67.11307$, $t_1 = -0.24943$, and $\mathrm{TTF}_0 = 3.17971$.

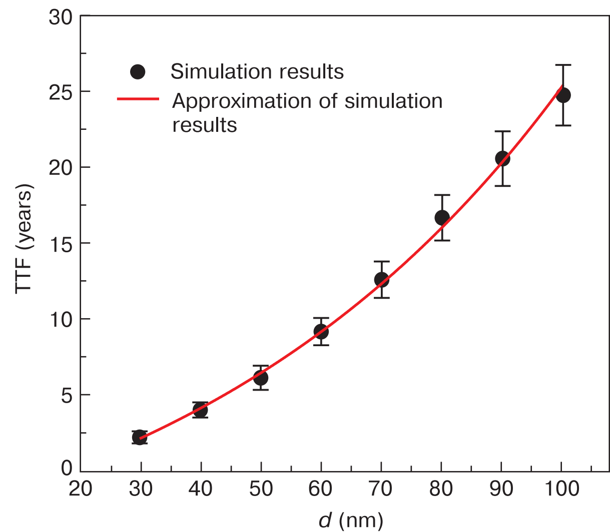

Figure 5. TTF as a function of distance between copper lines (at constant D, T and k)

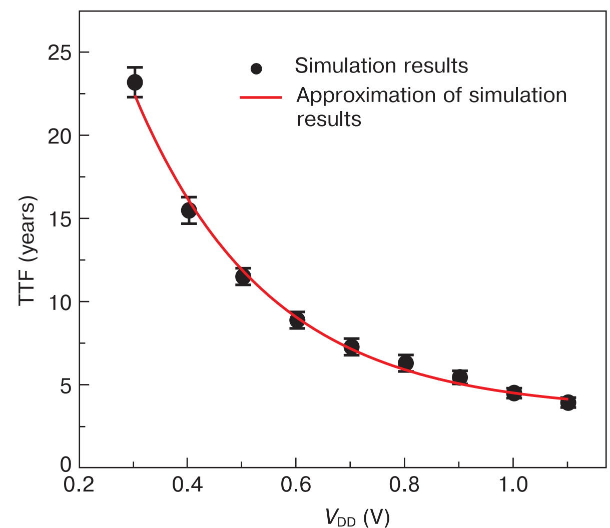

Figure 6. TTF as a function of power voltage V_{DD} (the other line being grounded) at constant D, T and k

3. Conclusion

Thus this work reports a method for estimating the time to failure of a porous dielectric in VLSI systems that is based on the determination of the diffusion coefficient from experimental data and calculations within a mathematical model of ion distribution for a metallic barrier in the low-k dielectric between two nearby copper lines. Additionally the TTF was calculated as a function of the distance between two nearby copper lines and as a function of one line’s power voltage (the other line is grounded). These functions are showed to be exponential.

Further studies are planned for analyzing the change in the TTF with a periodic signal being supplied to one line (the other line is grounded) as well as the TTF as a function of integrated circuit topology geometry.

References

1. International Technology Roadmap for Semiconductors (ITRS) Interconnect. 2020. https://irds.ieee.org/editions/2020
2. Gonella R. Key reliability issues for copper integration in damascene architecture. *Microelectronic Engineering*. 2001; 55(1-4): 245–255. https://doi.org/10.1016/S0167-9317(00)00454-8
3. Lloyd J.R., Murray C.E., Ponoth S., Cohen S., Liniger E. The effect of Cu diffusion on the TDDB behavior in a low-k interlevel dielectrics. *Microelectronics Reliability*. 2006; 46(9–11): 1643–1647. https://doi.org/10.1016/j.microrel.2006.08.003
4. Chen F., Bravo O., Chanda K., McLaughlin P., Sullivan T., Gill J., Lloyd J., Kontra R., Aitken J. A comprehensive study of low-k SiCOH TDDB phenomena and its reliability lifetime model development. In: *Proc. of the Intern. Reliability Physics Symposium*. 26-30, March 2006. New York: IEEE; 2006. P. 46–53. https://doi.org/10.1109/RELPHY.2006.251190

5. Suzumura N., Yamamoto S., Kodama D., Makabe K., Komori J., Murakami E., Maegawa S., Kubota K. A new TDDB degradation model based on Cu ion drift in Cu interconnect dielectrics. In: *Proc. of the Intern. Reliability Physics Symposium*. 26–30, March 2006. New York: IEEE; 2006. P. 484–489. https://doi.org/10.1109/RELPHY.2006.251266

6. Tan T.L., Gan C.L., Du A.Y., Cheng C.K. Effect of Ta migration from sidewall barrier on leakage current in Cu/SiOCH low-k dielectrics. *Journal of Applied Physics*. 2009; 106(4): 043517. https://doi.org/10.1063/1.3202387

7. Huang X., Sukharev V., Qi Z.-D., Kim T.-Y., Tan S. X.-D. Physics-based full-chip TDDB assessment for BEOL interconnects. In: *Proc. of the 53rd Annual Design Automation Conference 2016 – DAC '16*. 05–09, June 2016. Austin, USA: IEEE; 2016. https://doi.org/10.1145/2897937.2898062

8. Groove A.S. Physics and Technology of Semiconductor Devices. Hoboken, NJ, USA: Wiley, 1967.

9. Valeev A.S., Krasnikov G.Yu. Manufacturing technology of intra- and interchip interconnects for modern ULSIs: Review and concepts of development. *Russian Microelectronics*. 2015; 44(3): 154–172. https://doi.org/10.1134/S1063739715030087

10. Yang L.Y., Zhang D.H., Li C.Y., Liu R., Wee A.T.S., Foo P.D. Characterization of Cu/Ta/ultra low-k porous polymer structures for multilevel interconnects. *Thin Solid Films*. 2004; 462–463: 182–185. https://doi.org/10.1016/j.tsf.2004.05.071

11 Kuo Y.-L., Lee H.-H., Lee C., Lin J.-C., Shue S.-L., Liang M.-S., Daniels B.J. Diffusion of copper in titanium zirconium nitride thin films. *Electrochemical and Solid-State Letters*. 2004; 7(3): C35–C37. https://doi.org/10.1149/1.1644355